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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/659,584	09/11/2000	Hideo Aizawa	04329.2405	4490

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FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER LLP
1300 I STREET, NW
WASHINGTON, DC 20005

EXAMINER	
BARNES, CRYSTAL J	
ART UNIT	**PAPER NUMBER**
2121	5

DATE MAILED: 03/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/659,584	AIZAWA ET AL.	
	Examiner	Art Unit	
	Crystal J. Barnes	2121	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 September 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 September 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3,4*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 14 March 2001 is a duplicate of the information disclosure statement submitted on 11 September 2000. The submissions are in compliance with the provisions of 37 CFR 1.97. However, only one information disclosure statement is being considered by the examiner.

Drawings

3. The drawings are objected to because the control signal issued by test master model for controlling the LSI model in figure 1 should be unidirectional (see control signal issued by LSI model to memory model); "TEST_MODO" in figure 2 should be "TEST_MODE" (see page 11 line 1). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid

abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

4. The disclosure is objected to because of the following informalities: "TEST_ADDR" on page 11 lines 7, 9, 12 and "TEST_ADDRESS" in figure 2 have both been used to designate test address information. Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 2, 5-7, 10-12 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over USPN 6,053,948 to Vaidyanathan et al. in view of USPN 4,617,660 to Sakamoto.

As per claim 1, the Vaidyanathan et al. reference discloses a method of simulating an operation of a memory, comprising the steps of: simulating a read/write operation (see column 7 lines 15-20, "read/write") corresponding to a location (see column 6 lines 27-31, "memory location") specified by a first bit set of a memory address (see column 9 lines 44-45, "memory model address 301") including a plurality of bits ("set of bits"), using a memory model (see column 5 lines 51-56, "memory model 215") describing the operation of the memory ("physical memory device"); and generating an error in the read/write operation of the memory model (see column 16 lines 44-48, "error ... circuit model 200") in accordance with a value of a second bit set of the memory address by making a change to one of write data to be written to the memory model and read data read therefrom, the second bit set being not used for the simulation of the read/write operation using the memory model.

The Vaidyanathan et al. reference does not expressly disclose generating an error in the read/write operation of the memory model in accordance with a value of a second bit set of the memory address by making a change to one of write data to be written to the memory model and read data read therefrom.

The Sakamoto reference discloses

(see column 3 lines 27-31, "The MU includes an error detecting circuit for detecting errors in read and write data ... error correcting circuit for automatically correcting the detected error.")

(see column 3 lines 33-40, "... selecting one of the write data from the write data register 1 and rewrite data from an inversion and selection unit 10 ...")

(see column 4 lines 14-15. "The MU includes registers ... for storing the bit position of the hard error ...")

(see column 4 lines 20-25, "... selects one of read data from the read data registers 6 and 7 ... error detecting circuit 9 for detecting errors and for producing ECC and/or to the inversion and selection circuit 10, which functions to correct an error bit by inverting data applied thereto.")

(see column 5 lines 11-21, "... ECC of 7 bits, the error detecting circuit 9 and the inversion and selection circuit 10 can automatically correct an error of 1 bit and detect an error of 2 bits ... a 1 bit error indicating bit 14-1-1 ... a 2 bit error indicating bit 14-1-2 ...")

(see column 5 lines 43-47, "... memory error is 1 bit error or 2 bit error ... contents in the 1 bit error indicating bit 14-1-1 and in the 2 bit error indicating bit 14-1-2 ...")

(see column 8 lines 40-46, "If there is a 1 bit error ... error bit is corrected by inverting it at the inversion and selection circuit 10, depending upon the error bit position information ...")

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the method and apparatus using a memory model taught by the Vaidyanathan et al. reference with the memory unit taught by the Sakamoto reference to illustrate a particular memory model that can be used in electronic design automation systems.

One of ordinary skill in the art would have been motivated to illustrate a particular memory model that can be used in electronic design automation systems to allow designers to simulate the operation of memory circuits with different stimuli using descriptions of the memory circuits (see Vaidyanathan et al. column 1 lines 25-28).

As per claim 2, the Sakamoto reference discloses the second bit set of the memory address includes error address information (see column 7 lines 24-28, "error bit position information") for specifying an error generating address (see column 4 lines 14-15, "bit position") and error mode information (see column 5 lines 42-43, "status of memory error") for specifying a content of error generation (see

column 5 lines 43-46, "1 bit error or 2 bit error"), and the error generating step comprises: a step of detecting whether a value of the first bit set of the memory address (see column 4 lines 56-60, "error bit position indicating bits 14-4") and a value specified by the error address information (see column 4 lines 56-60, "error bit position information") coincide with each other; and a step of reversing at least one bit (see column 5 lines 15-21, "1 bit error indicating bit 14-1-4, 2 bit error indicating bit 14-1-2") of one of the write data and the read data (see column 5 lines 1-3, "read data") in accordance with the error mode information ("status of memory error") when the value of the first bit set ("error bit position indicating bits 14-4") and the value specified by the error address information ("error bit position information") coincide with each other.

As per claim 5, the rejection of claim 1 is incorporated and further claim 5 contains limitations recited in claim 1; therefore claim 5 is rejected under the same rationale as claim 1.

As per claim 6, the rejection of claim 1 is incorporated and further claim 6 contains limitations recited in claim 1; therefore claim 6 is rejected under the same rationale as claim 1.

As per claim 7, the rejection of claim 2 is incorporated and further claim 7 contains limitations recited in claim 2; therefore claim 7 is rejected under the same rationale as claim 2.

As per claim 10, the rejection of claim 1 is incorporated and further claim 10 contains limitations recited in claim 1; therefore claim 10 is rejected under the same rationale as claim 1.

As per claim 11, the rejection of claim 1 is incorporated and further claim 11 contains limitations recited in claim 1; therefore claim 11 is rejected under the same rationale as claim 1.

As per claim 12, the rejection of claim 2 is incorporated and further claim 12 contains limitations recited in claim 2; therefore claim 12 is rejected under the same rationale as claim 2.

As per claim 15, the rejection of claim 1 is incorporated and further claim 15 contains limitations recited in claim 1; therefore claim 15 is rejected under the same rationale as claim 1.

7. Claims 3, 4, 8, 9, 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over USPN 6,053,948 to Vaidyanathan et al. in view of USPN

4,617,660 to Sakamoto as applied to claims 1, 2, 5-7, 10-12 and 15 above, and further in view of USPN 5,337,317 to Takamisawa et al.

As per claim 3, neither the Vaidyanathan et al. reference nor the Sakamoto reference disclose the memory model describes an operation of a nonvolatile semiconductor memory to which write data and an error correction code thereof are written in units of data size so as to correspond to each other, and the method further comprises a step of simulating an error correcting operation of a memory controller for controlling the nonvolatile semiconductor memory, based on the read data and the error correction code, using an LSI model describing an operation of the memory controller.

The Takamisawa et al. reference discloses

(see column 3 lines 30-38, "The semiconductor integrated memory circuit ... PROM 104 ... read signal instructing a data reading ... program signal instructing a data writing ...")

(see column 3 lines 47-53, "The data bit section 104 A and the check bit section 104B ... error correction circuit 105 ... read-out data bit set ... read-out check bit set ...")

(see column 4 lines 52-61, "The error correction circuit 104 ... four data bits ...four check bits ... corrected data bits if an error of one bit occurs ...")

(see column 6 lines 37-43, "... a check bit set stored at a memory location ... inverting the most significant bit ... data bit set constitutes the check bit set for the data bit set stored at a memory location ...")

(see column 7 lines 8-14, "When the program signal is active ... data bits ... are written or programmed into a data bit cell set ...")

(see column 7 lines 15-22, "... when the program signal is active ... data bits ... are written or programmed into a check bit cell set ...")

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to further modify the memory model taught by the Vaidyanathan et al. reference with the memory unit taught by the Sakamoto reference and the semiconductor integrated memory circuit taught by the Takamisawa et al. reference to illustrate specific functions of a memory model that can be used in electronic design automation systems.

One of ordinary skill in the art would have been motivated to illustrate specific functions of a memory model that can be used in electronic design

automation systems to verify the functionality of memory design before the memory is built through simulation.

As per claim 4, the Sakamoto reference discloses the error generating step includes a first error mode (see column 5 lines 42-56, "1 bit error") for making a change to one of the write data to be written to the memory model and the read data read therefrom (see column 5 lines 38-41, "inversion and selection circuit 10") within the number of error correctable bits ("1 bit") using the error correction code (see column 5 lines 15-21, "error detection signal") and a second error mode (see column 5 lines 42-56, "2 bit error") for making a change thereto by the number of bits exceeding the number of error correctable bits ("2 bits"), one of the first error mode ("1 bit error") and the second error mode ("2 bit error") being chosen in accordance with the value of the second bit set of the memory address (see columns 10-11 lines 65-4, "error detection and error correction capabilities").

As per claim 8, the rejection of claim 3 is incorporated and further claim 8 contains limitations recited in claim 3; therefore claim 8 is rejected under the same rationale as claim 3.

As per claim 9, the rejection of claim 4 is incorporated and further claim 9 contains limitations recited in claim 4; therefore claim 9 is rejected under the same rationale as claim 4.

As per claim 13, the rejection of claim 3 is incorporated and further claim 13 contains limitations recited in claim 3; therefore claim 13 is rejected under the same rationale as claim 3.

As per claim 14, the rejection of claim 4 is incorporated and further claim 14 contains limitations recited in claim 4; therefore claim 14 is rejected under the same rationale as claim 4.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respect to modeling memory in general:

USPN 6,539,503 B1 to Walker

USPN 6,144,930 to Kinzelman

USPN 6,012,157 to Lu

The following patents are cited to further show the state of the art with respect to memory error correction in general:

USPN 4,800,563 to Itagaki et al.

JPPN 57-66597 A to MASUDA

JPPN 56-11700 A to KIKUCHI

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Crystal J. Barnes whose telephone number is 703.306.5448. The examiner can normally be reached on Monday-Friday alternate Mondays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Anil Khatri can be reached on 703.305.0282. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

cjb
5 March 2004

RAMESH PATEL
PRIMARY EXAMINER